Memory Access Analysis and Optimization for Ultra High Definition Video Coding

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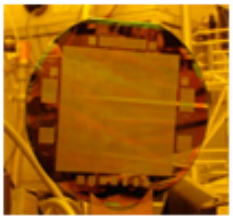
More Pixels

EE Times: Semi News

Record CCD image sensor has 111 million pixels

Peter Clarke
EE Times
(06/19/2006 9:46 H EDT)



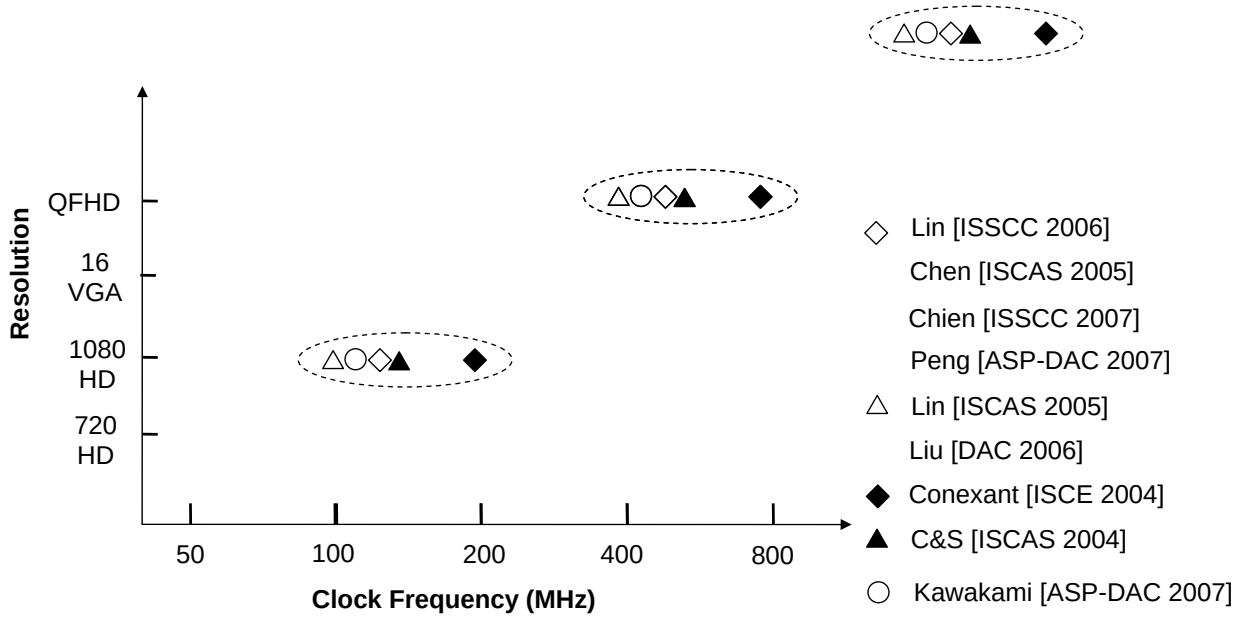
LONDON — Dalsa Semicon
sensor with more than 111 n
claims the 4 x 4-inch charge
10,560 x 10,560 pixels, is th
image sensor and the first to
barrier.

NHK Proposes UHD TV Broadcast

- Super HiVision 7680x4320 pixels at 60 fps (16xHDTV)
- Baseband signal is 24 Gbps. compressed to 250 Mbps for transmission.
- HDTV signals are 1.5 Gbps for baseband and 20 Mbps for compressed signals.
- High Performance compression / decompression and transmission / storage are needed

Applications

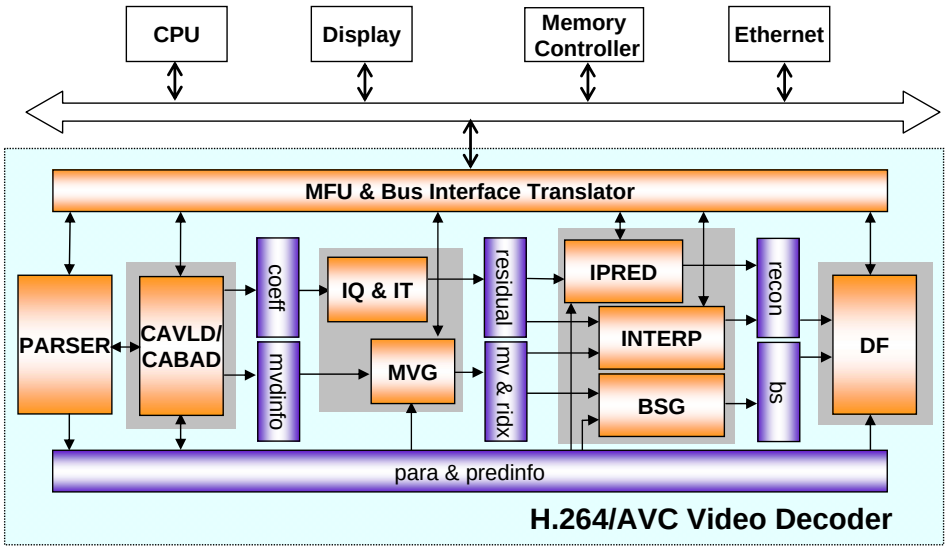
State-of-the-art H.264/AVC Decoders



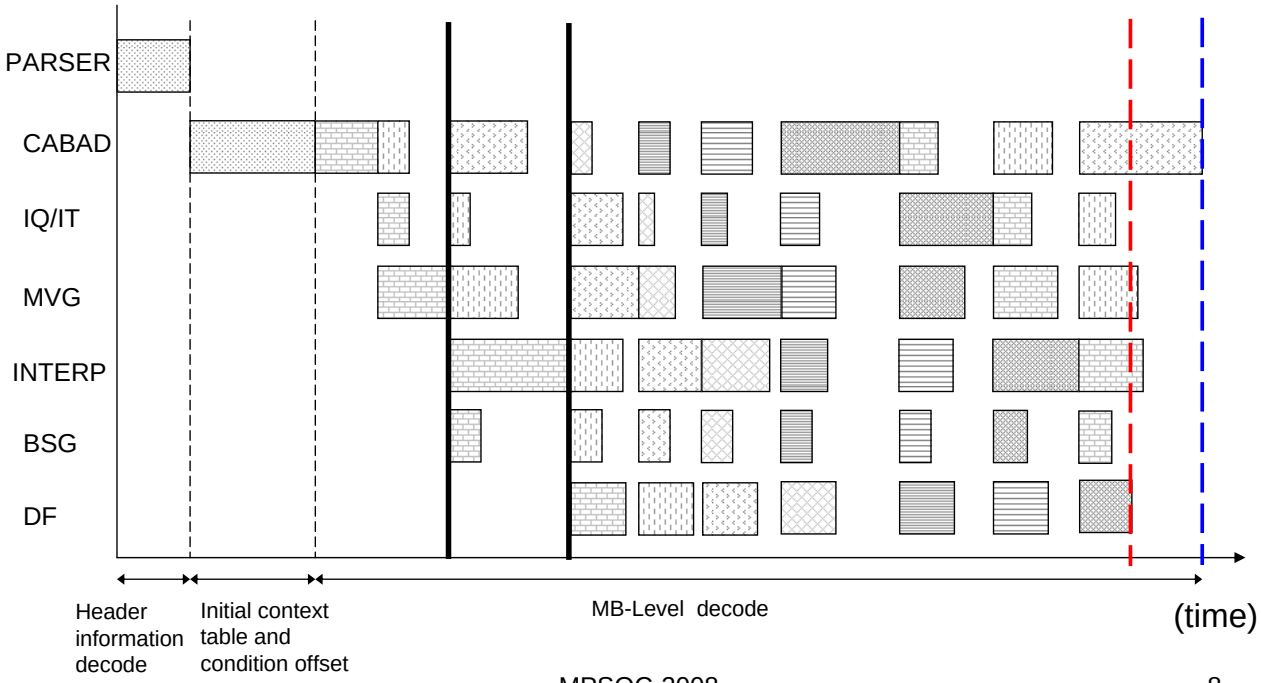
Design Spec

- Real-time (30fps) Decoding of QFHD (4x1080pHD) H.264/AVC Video
- Running under 200MHz, Using a 128-bit Bus
- Timing Budget: 200 cycles per macro-block (MB)

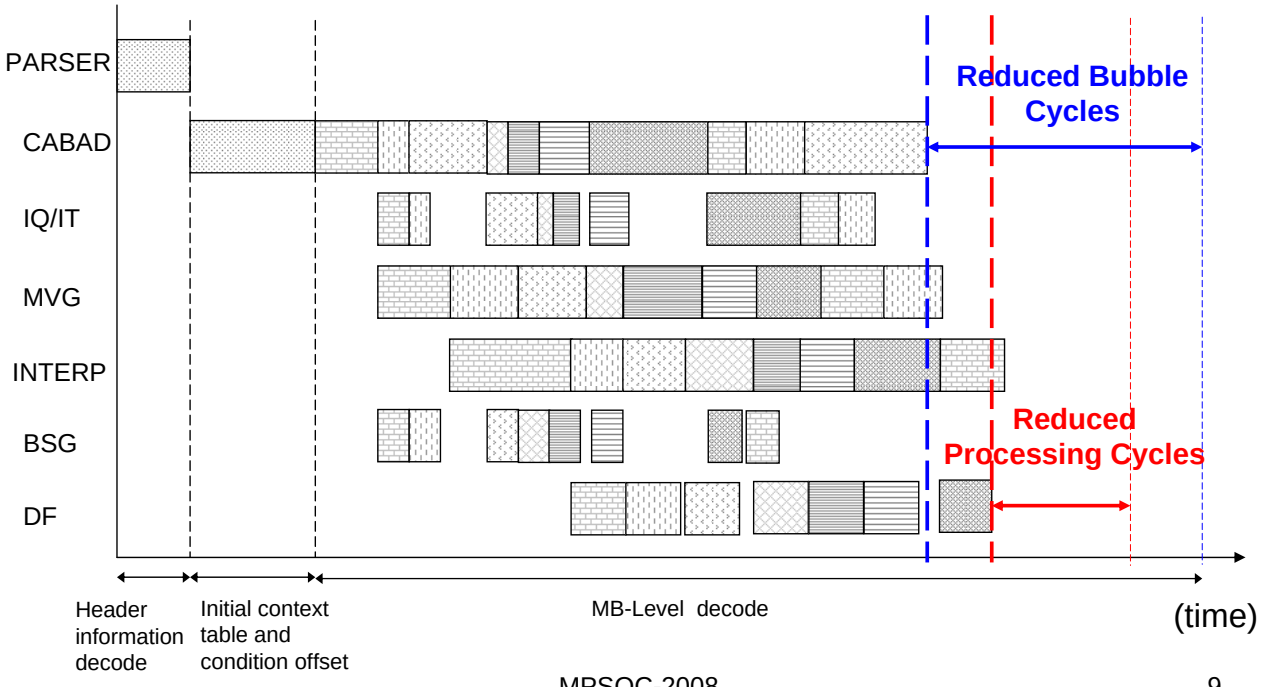
Pipeline Architecture



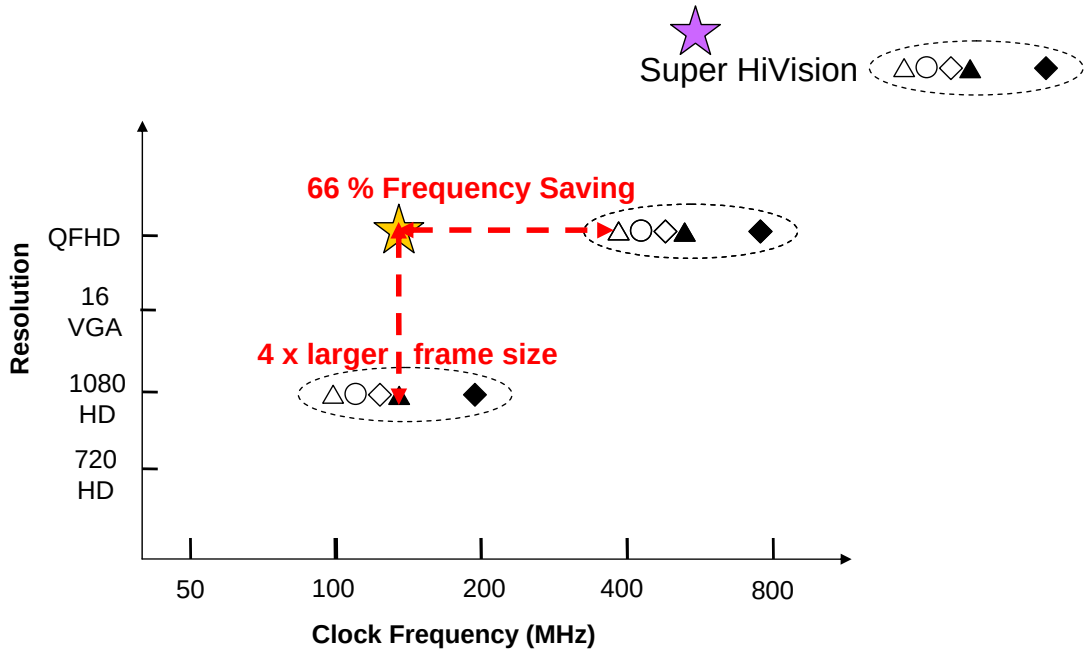
MB-Based Pipeline Scheduling



Adaptive Pipeline Scheduling

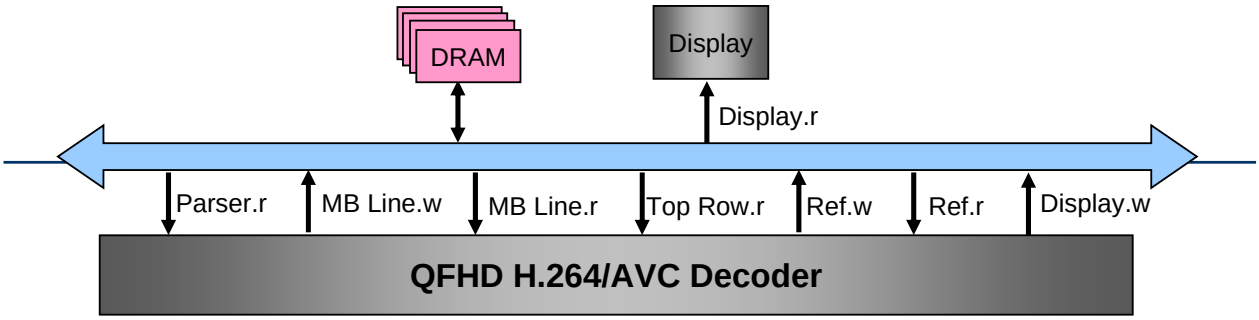


NTHU QFHD H.264/AVC Decoder



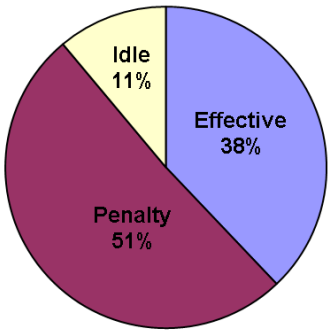
Next Bottleneck

- We have adequate performance in the decoding pipe for up to 16xFullHD
- External memory access becomes a problem
  - Trade-Off Between Memory Traffic and Buffer Size
  - DRAM Access Penalty Depends on Memory Allocation and Access Pattern



	Data Cycle (Effective)		Bus Cycle (Effective + Penalty)		Utilization
	Million Cycles	%	Million Cycles	%	%
Parser read	0.05	0.2	0.13	0.2	42.0
MB Line write	1.54	4.6	1.80	2.3	85.6
MB Line read	1.54	4.6	2.88	3.6	53.5
Top Row read	0.98	2.9	4.85	6.1	20.1
Ref. write	6.41	19.1	10.81	13.6	59.3
Ref. read	7.40	21.5	13.36	16.9	54.9
Display write	8.61	25.6	36.31	45.8	23.7
Display read	7.26	21.6	9.13	11.5	79.5

To Reduce Bus Traffic

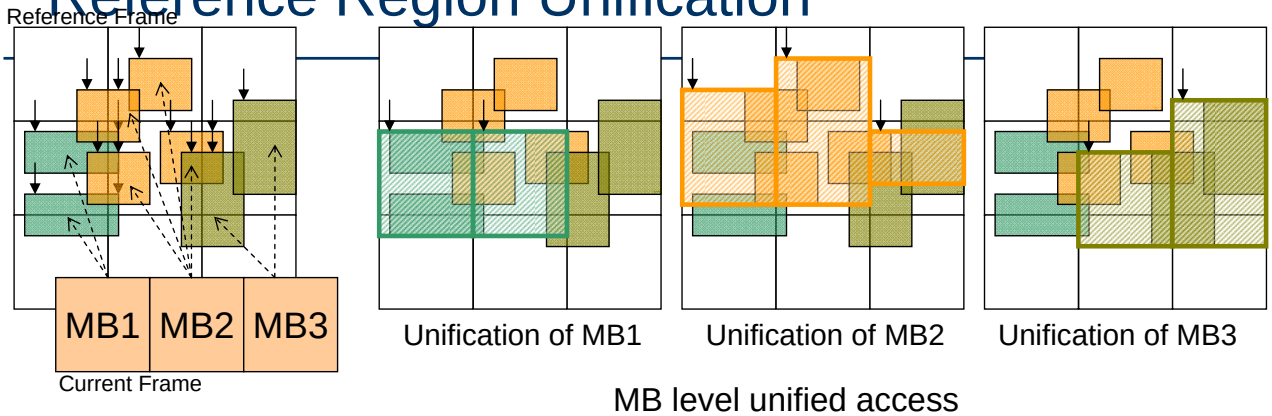


1. Reduce effective cycles
- **Data compression**

2. Reduce DRAM penalty cycles
- **Better address-mappings**
- **Scheduling according to DRAM status**
- **Pre-handling of DRAM accesses**

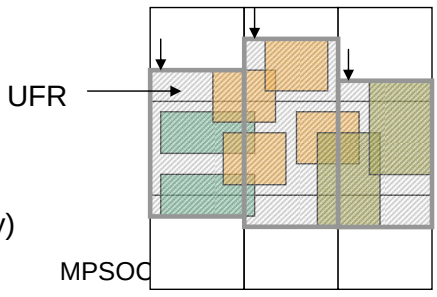
3. Reduce idle cycles
- **Prioritization according to BW requirements and access urgencies**

Motion Compensator Reference Region Unification



Straightforward access
(14 burst access penalties)

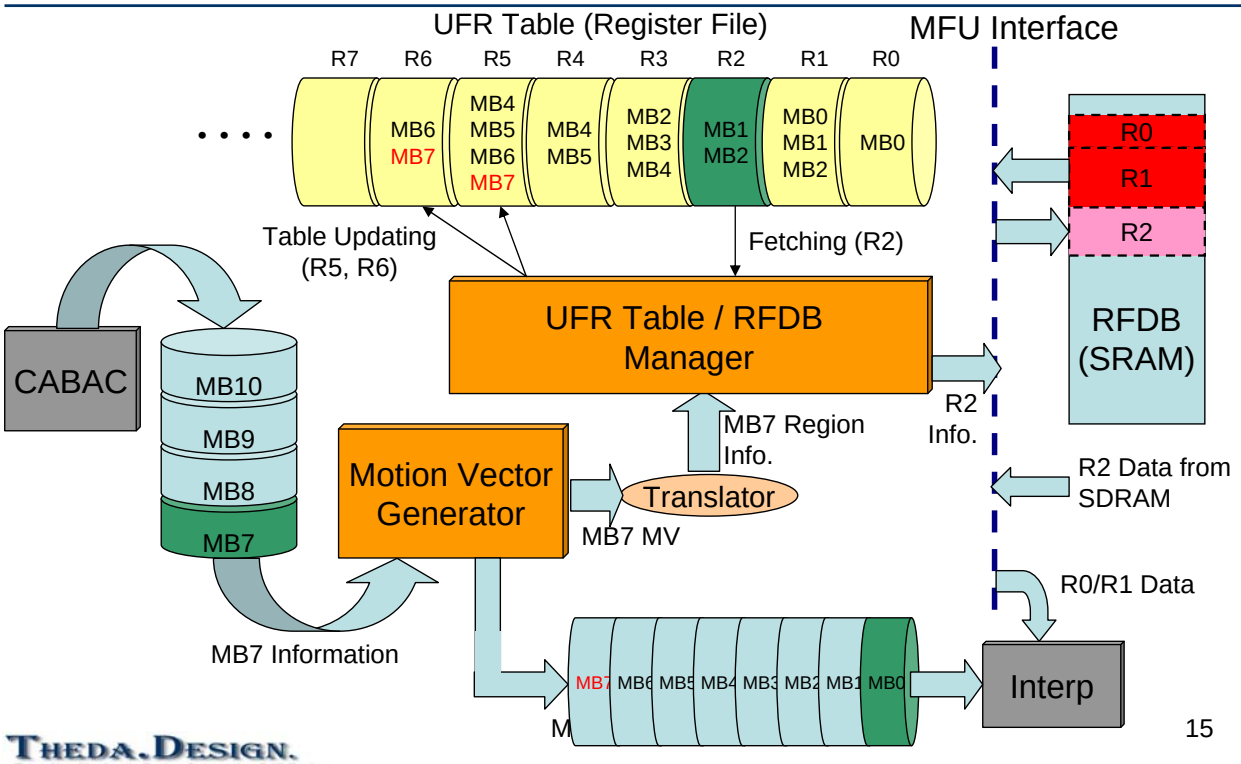
MB level unified access
(7 burst access penalties)



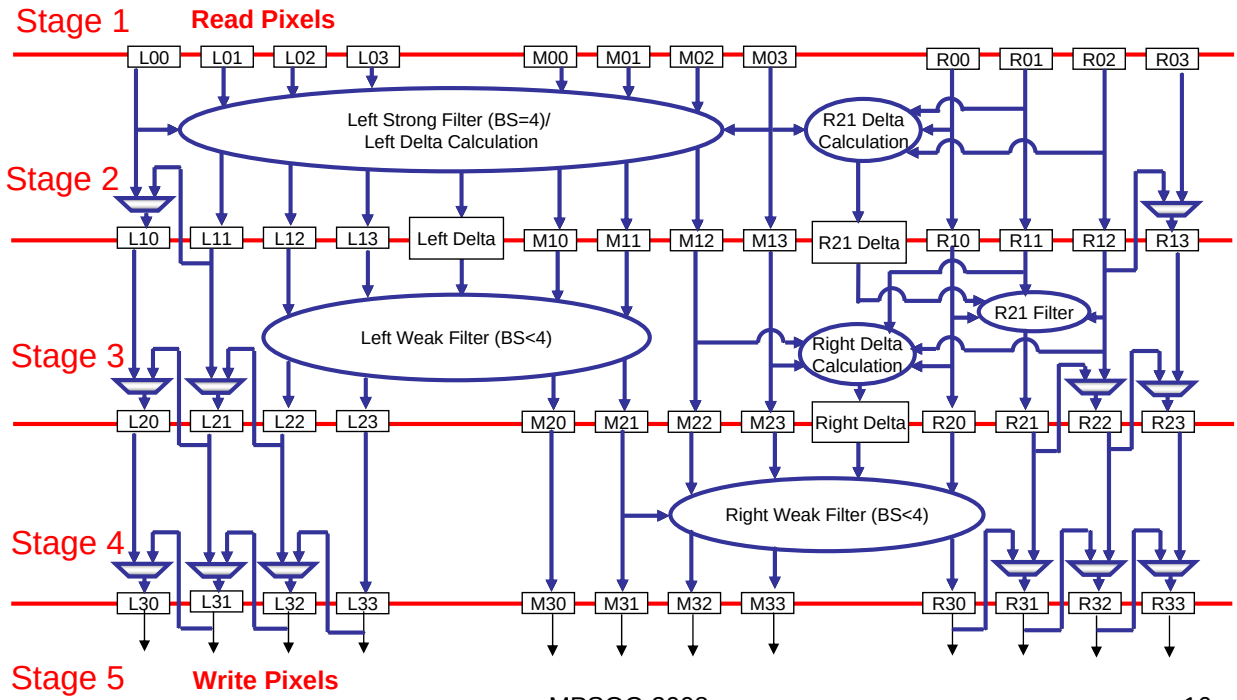
MB-row level unified access (3 burst access penalties)

↓ : Burst initial (burst access penalty)

Reference Frame Pre-Fetching

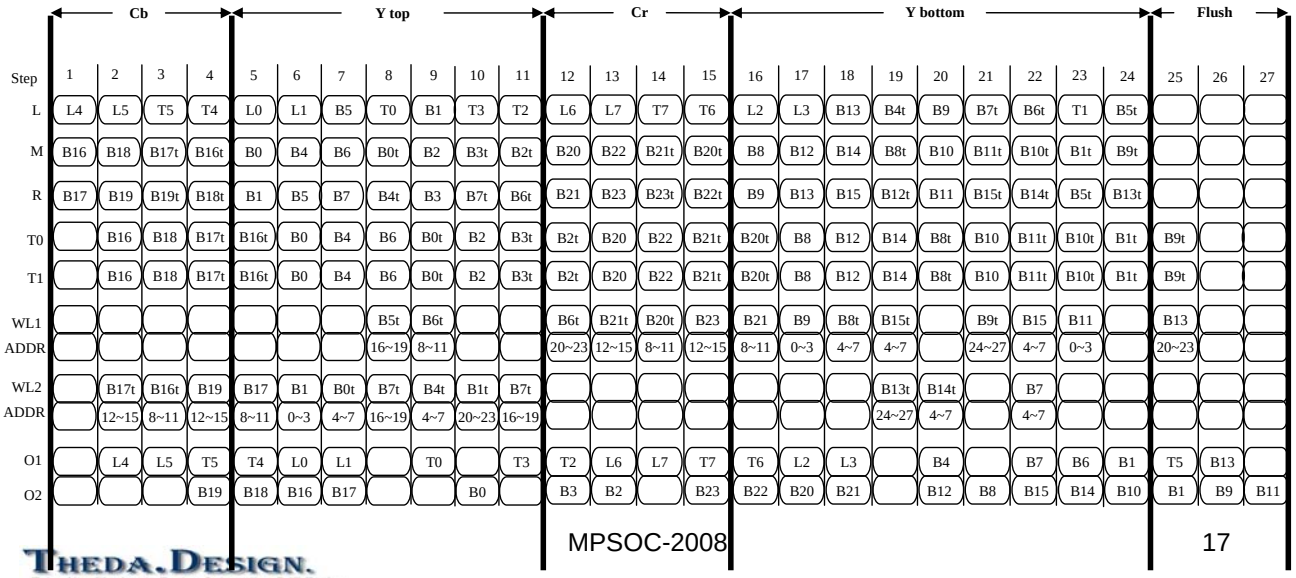


5-Stage Dual Deblocking Filter

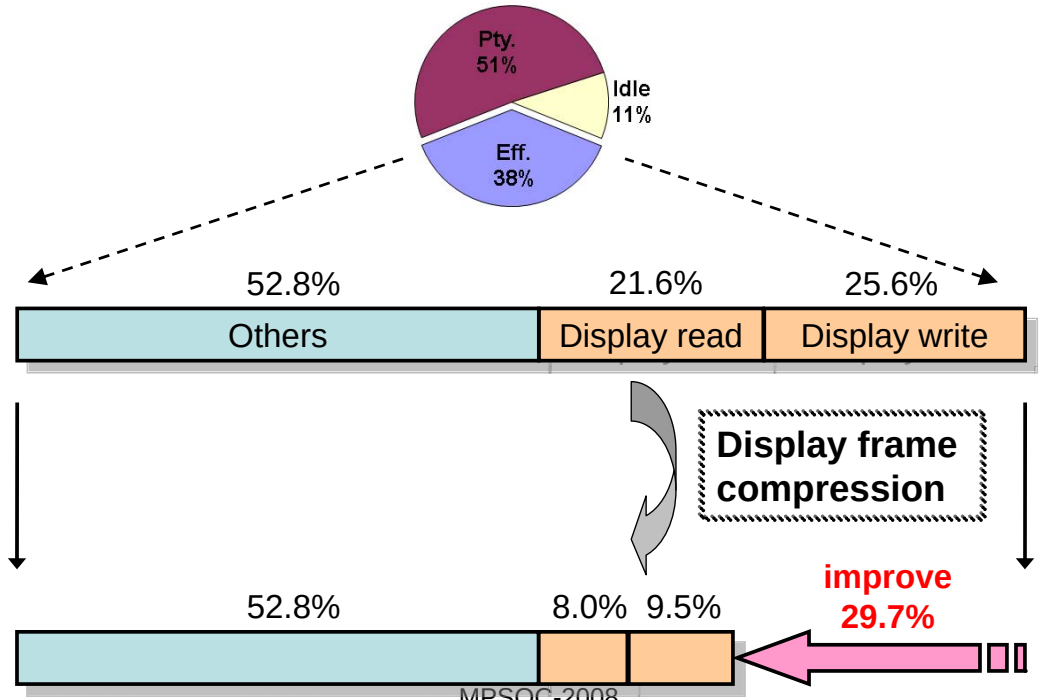


Perfect DF Scheduling

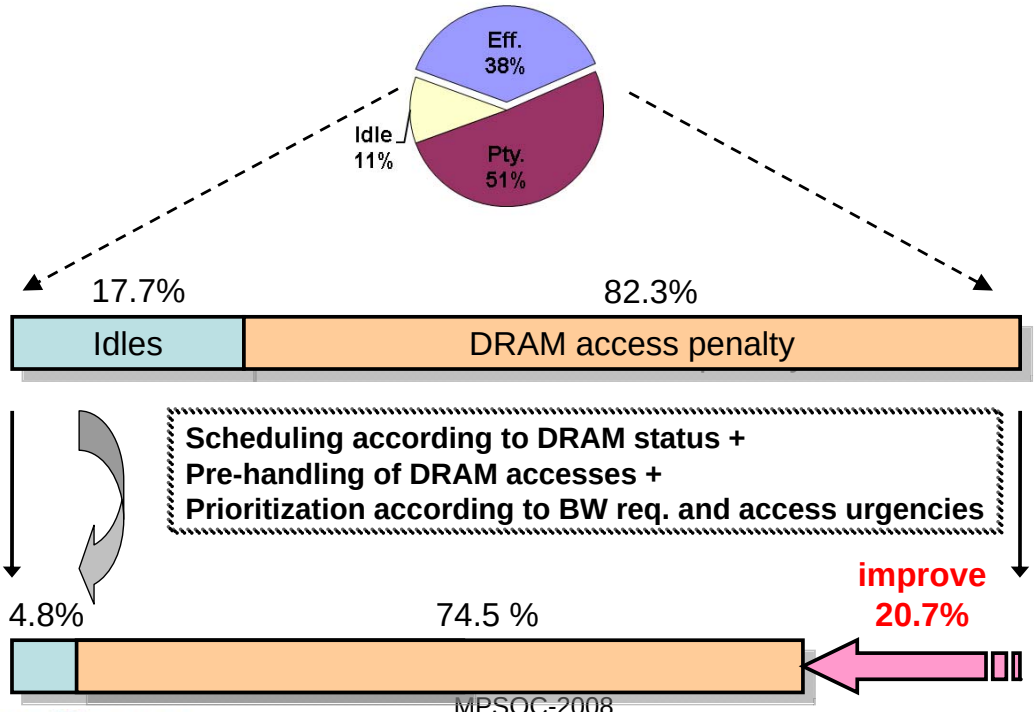
- 96 Filtering cycles with 100% utilization of the edge filter
- The last 8 flush cycles can be overlapped with next MB



Effective Traffic Reduction



Penalty and Idle Reduction



Increased BW Utilization

	Utilization Before	Utilization After
	%	%
Parser read	42.0	48.1
MB Line write	85.6	89.4
MB Line read	53.5	59.3
Top Row read	20.1	26.2
Ref. write	59.3	66.0
Ref. read	54.9	58.9
Display write	23.7	30.2
Display read	79.5	85.7

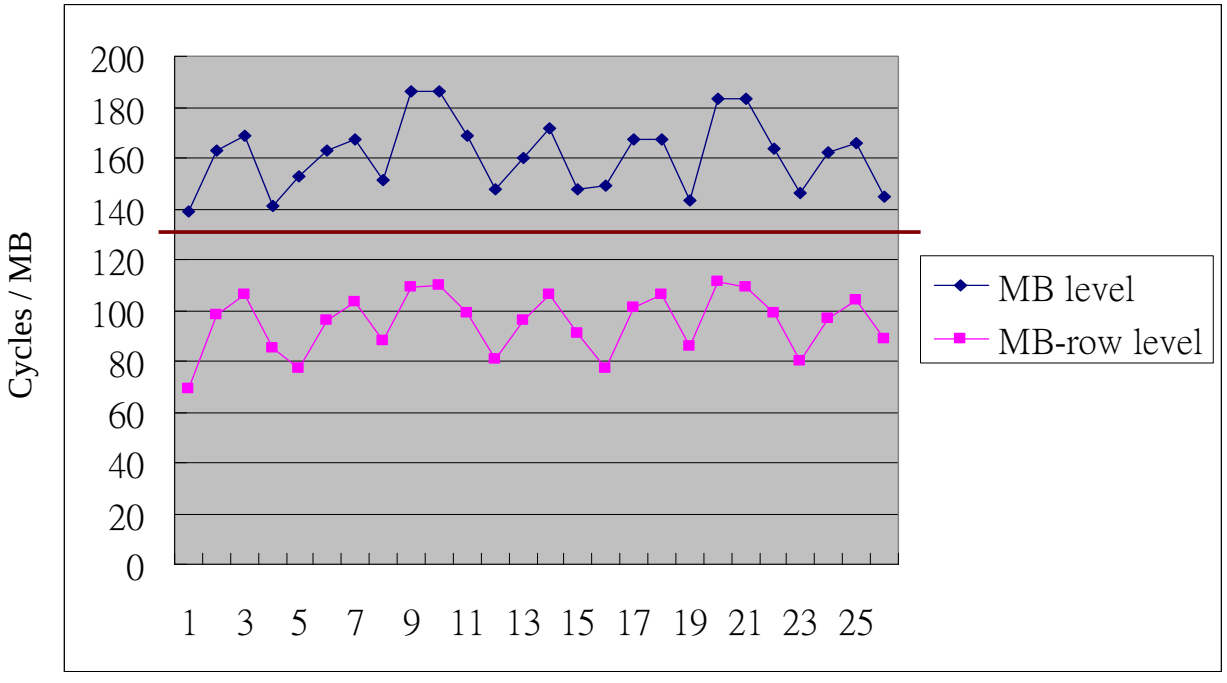
NOTE:
The previous 2 slides assume *independent* discussions of different techniques, but in fact the size of DRAM penalty should depend on the size of effective traffic

Memory Traffic Sim. Result (1/2)

Sequence (IBBBP, sr64, ref4)	Cycle Count of Data Fetch			
	Ref. Window	Straight-forward (Software Simulation)	MB Level Unification (Software Simulation)	Proposed MB-row Level Unification (RTL Simulation)
tractor	1048	1323	202	112
bluesky		1227	161	98
pedestrian		1129	171	111
sunflower		1340	181	100
rushhour		1103	178	111
station		1284	180	101

Working on 128bits bus, with simulated burst access penalty = 20 cycles

Memory Traffic Sim. Result (2/2)



Summary

- Hardwired H.264/AVC Video Decoder Pipeline Capable of Super HiVision (16xFullHD) Performance
- External Memory Allocation and Access Critical
  - MB-based Column Allocation
  - Reference Region Unification
  - Pre-Fetching
  - Perfect Scheduling in both IP and Bus/Memory